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ITO with embedded silver grids as transparent conductive electrodes for large area organic solar cells

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Abstract

In this work, development of semi-transparent electrodes for efficient large area organic solar cells (OSCs) has been demonstrated. Electron beam evaporated silver grids were embedded in commercially available ITO coatings on glass, through a standard negative photolithography process, in order to improve the conductivity of planar ITO substrates. The fabricated electrodes with embedded line and square patterned Ag grids reduced the sheet resistance of ITO by 25% and 40%, respectively, showing optical transmittance drops of less than 6% within the complete visible light spectrum for both patterns. Solution processed bulk heterojunction OSCs based on PTB7:[70]PCBM were fabricated on top of these electrodes with cell areas of 4.38 cm^2, and the performance of these OSCs was compared to reference cells fabricated on pure ITO electrodes. The Fill Factor (FF) of the large-scale OSCs fabricated on ITO with embedded Ag grids was enhanced by 18% for the line grids pattern and 30% for the square grids pattern compared to that of the reference OSCs. The increase in the FF was directly correlated to the decrease in the series resistance of the OSCs. The maximum power conversion efficiency (PCE) of the OSCs was measured to be 4.34%, which is 23% higher than the PCE of the reference OSCs. As the presented method does not involve high temperature processing, it could be considered a general approach for development of large area organic electronics on solvent resistant, flexible substrates.

Keywords: embedded metal grids in ITO, transparent conductive electrodes, large area organic solar cells, low ITO sheet resistance, lithography processed silver grids, device series resistance

(Some figures may appear in colour only in the online journal)

1. Introduction

On a laboratory scale, the Power Conversion Efficiency (PCE) of Organic Solar Cells (OSCs) has successfully crossed double-digit figures in recent time, reaching record PCE of 13.2% [1–3], however, the large area fabrication of OSCs still contains several challenges. Some of these challenges are related to the technical aspects of up-scaling devices, such as non-uniform layers and contamination issues, which can be solved through well controlled processing methods. Another reason for the still relatively low performance of large area OSCs is due to the semi-transparent electrodes used in the fabrication process [4, 5]. The resistance of the semi-transparent electrodes leads to a pronounced increase in the series resistance of the up-scaled devices, which in turn leads to a performance decrease of the OSCs [6–9].

Despite its brittleness, Indium-Tin-Oxide (ITO) is widely used as the semi-transparent electrode material in the

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fabrication of OSCs due to its relatively high conductivity and transparency, which leads to high performance in lab-scale scale devices [10]. However, when developing devices on the large scale, the resistance of the ITO electrodes becomes relevant [11], as it causes the developed OSCs to experience significant drops in device efficiency. Increasing the thickness of the ITO layer can decrease its sheet resistance, but it also reduces the optical transmittance at the same time [12], and thus the number of photons reaching the active layer in cells. Replacing ITO electrodes by integrating current collecting metal grids with conductive polymers, or by using ultrathin metal films, have been reported earlier [13–16], however, these approaches suffer from either a high sheet resistance, or a low optical transmittance compared to ITO [17–20].

Several investigations on decreasing the sheet resistance of ITO electrodes without losing a significant part of their optical transmittance have been made for the developing efficient, large area OSCs [21]. It has for example been reported that introducing an ultra thin metal layer, or thin metal grids on top or in between layers of ITO reduces the sheet resistance of ITO remarkably [17, 22–25]. Fabricating metal grids directly on top of ITO is capable of reducing the over all resistance of ITO [26]. However, the thickness of metal grids in this method remains critical in these thin-film devices. In terms of resistivity, it is desirable to have metal grids as thick as possible on the ITO layer as it lowers the resistance of the ITO electrode significantly. On the other hand, during the organic devices fabrication, thin organic layers may not fully cover the thicker metal grids on ITO, which may lead to electrically shorted devices [22, 27].

Jeong *et al*, have reported on highly conductive inkjet printed ITO/Silver grids/ITO transparent electrodes [28], while Guillen *et al*, have investigated Metal/ITO and ITO/Metal/ITO structures prepared by sputter deposition [29]. However, in these reports, the optical transmittance of the electrodes drop significantly in the visible light range [28, 29]. Also, the post-deposition annealing temperatures for the investigated structures were as high as 350 °C–450 °C [28, 29], which makes this approach unsuitable for substrates that cannot withstand such a high temperatures.

In this work, low temperature processed semi-transparent electrodes comprised of ITO with embedded Ag grids were produced, in order to develop highly conductive semi-transparent and planar electrodes suitable for large area OSCs. Ag grids were embedded using line and square patterns (see figures 3(a) and (b)) inside the ITO layer. It is demonstrated that embedding 70 nm Ag grids of line and square patterns in 100 nm thick ITO reduces the sheet resistance by 25% and 40%, respectively, while losing <6% of the original optical transmittance. The planar electrodes ensure a complete coverage of the organic layers during the device fabrication process. In order to demonstrate this, solution processed inverted bulk heterojunction OSCs based on PTB7:[70]PCBM with the cell area of 4.38 cm^2 were fabricated. The OSCs show improved Fill Factor (>50%) and exhibit a maximum PCE of 4.34%, which is 23% higher than the PCE of the reference OSCs fabricated on pure ITO electrodes.

2. Experimental

2.1. Fabrication of reference ITO electrodes

Photoresist (AZ5214E, Microchemicals GmbH, Germany) was spin coated on commercial ITO (100 nm) coated glass wafers (University wafers, USA) and baked at 90 °C for 1 min on a hot plate. Photoresist coated ITO wafers were patterned by a positive photolithography process using a Karl Suss MA 150 Aligner. Etching of ITO was performed in $HCl:HNO_3:H_2O$ (1:0.08:1) solution at 40 °C for 4 min—at the etch rate of approx. 0.5 nm s^{-1}. The photoresist was then stripped off by ultra-sonication in an Acetone bath for 10 min.

2.2. Embedding Ag grids in ITO

The key steps involved in entire process flow of embedding the Ag grids in ITO are shown in figure 1.

A thin layer of Bis(trimethylsilyl)amine (HMDS) was applied at 120 °C on the pre-patterned ITO electrodes as an adhesion promoter (pre-patterned electrodes, section 2.1). Photoresist (AZ5214E) was spin coated on the HMDS coated wafers and baked on a hot plate at 90 °C for 1 min. Line and square grid patterns were created on the photoresist coated pre-patterned ITO electrodes using a shadow mask and a negative lithography process.

Approx. 80 nm of ITO was etched away from the grid patterns by wet etching of the developed wafers in $HCl:HNO_3:H_2O$ (1:0.08:1) solution at 40 °C for 2 min 40 s at the etching rate of approx. 0.5 nm s^{-1}.

3 nm Titanium (Ti) was evaporated (as an adhesive layer) followed by 70 nm of Silver (Ag) on the patterned wafers by E-beam evaporation, using a base pressure of 5×10^{-5} mbar and deposition rates of 0.5 nm s^{-1} and 1 nm s^{-1}, respectively, without breaking the vacuum in between the layers. The remaining metal-coated photoresists was removed in a lift-off process in an Acetone bath by ultra-sonication for 20 min.

2.3. Characterization of the electrodes

The height profiles of the etched ITO surfaces were measured by a Dektak stylus profilometer. The sheet resistance of the electrodes was measured at multiple areas on a single sample using a homemade four-point probe measurement setup having spacing of 4.5 mm between the probes. AFM images were scanned using a Veeco Dimension 3100 scanning probe microscope. In order to record the transmittance spectra, the samples were illuminated (excluding the outer busbars) with a stabilized halogen light source (Thorlabs, SLS301) with a beam diameter of 16 mm, adjusted by a pinhole. Transmitted light was collected by an integrating sphere (Labsphere, RTC-060-SF) and recorded by spectrometer (Ocean Optics, Jaz).

2.4. Fabrication of OSCs

The fabricated wafers were cut into 30 × 30 mm substrates, which were cleaned stepwise with Extran industrial detergent, DI water, Acetone and Isopropanol for 10 min each in an ultrasonic water bath, and subsequently dried with Nitrogen

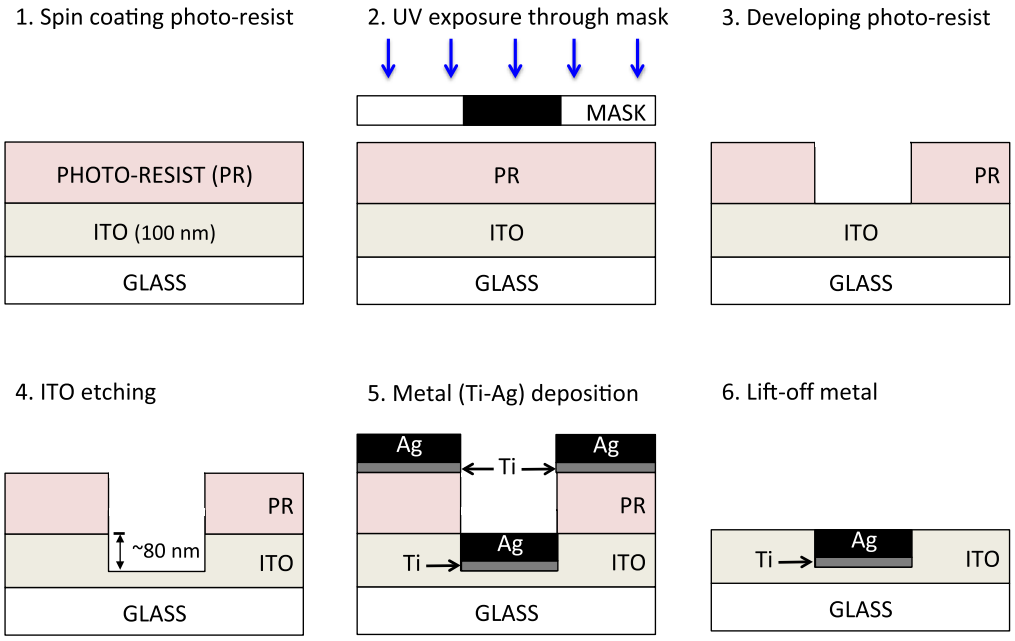

Figure 1. Highlights of the process of embedding 70 nm Ag grids in 100 nm thick ITO layer using photolithography: Step 1. Spin coating of photoresist on HMDS coated ITO wafers; Step 2. UV exposure of the photoresist using a shadow mask by negative photolithography; Step 3. Developing of the exposed photoresist in the developer (AZ351B) solution; Step 4. Partial etching of ITO in HCl:HNO_3:H_2O solution; Step 5. E-beam deposition of 3 nm Ti (adhesive layer) and 70 nm Ag grids on the etched ITO with photoresist on; Step 6. Lift-off of the excess metal and photoresist in Acetone bath.

(N_2). The plain ITO substrates were air plasma treated for 10 min.

The molecular structures of PTB7 (Molecular weight (GPC): >130 000 (Mw, PS Standard), Polydispersity (PDI): 2.5; 1-material, Canada) and [70]PCBM (Purity: >99%, Solenne BV, The Netherlands) are shown in figure 2. The solution blend of PTB7:[70]PCBM was prepared by dissolving PTB7 and [70]PCBM at a weight ratio of 1:1.5 respectively, in chlorobenzene, adding subsequently 3%v/v of 1,8-diiodooctane (DIO) to the solution. The solution was stirred overnight at room temperature. The patterned substrates were spin coated with Zinc oxide (ZnO) nanoparticles (Genes' Ink, France) at 1000 rpm for 60 s followed by annealing at 130 °C for 20 min on a hot plate. The solution blend of the active layer (PTB7:[70]PCBM) was spin coated at 1000 rpm for 2 min and dried in a slight vacuum (10^{-1} mbar) for 20 min. All sample fabrication steps were conducted in a N_2 filled glove box. Following the active layer, 8 nm of MoO_3 and 100 nm of Ag were thermally evaporated at a base pressure of 1×10^{-7} mbar with the growth rates of 0.02 nm s^{-1} and 0.05 nm s^{-1} respectively. The samples were loaded directly from the N_2 glove box into the evaporation chamber.

2.5. Characterization of OSCs

Current density–Voltage (JV) characteristics of the fabricated OSCs were measured by using a class AAA solar simulator (Sun 3000, Abet Technologies Inc., USA) having the lamp intensity of 100 mW cm^{-2}. JV characteristics under dark and illumination were measured by applying voltage sweep of +2 to −1 V using a 2400 source measure unit (Keithley Instruments Inc., USA).

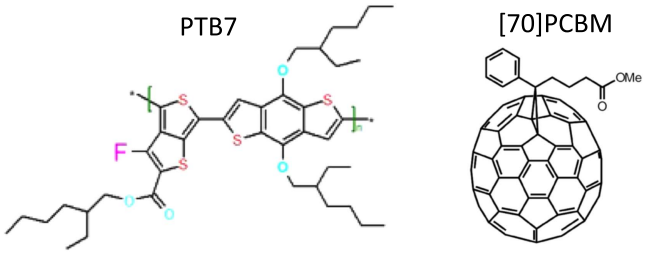

Figure 2. The molecular structures of PTB7 (donor) [30] and [70]PCBM (acceptor). Reproduced with permission from [31].

3. Results and discussion

Figures 3(a) and (b), respectively, show the schematic illustrations of the line and square patterned Ag grids embedded in the ITO substrates. The widths (w) of the grid lines are 120 μm and the outer busbars are 500 μm wide in both the cases. Figure 3(c) shows the height profile of the etched grid region on ITO after stripping off the photoresist, displaying that the 2 min 40 s etching removes approx. 80 nm of ITO. Figure 3(d) shows an optical microscope image of an embedded Ag grid line in ITO.

3 nm of Ti is present as an adhesion layer between the etched ITO and the evaporated 70 nm Ag, in order to protect the Ag layer from peeling off during the different subsequent process steps.

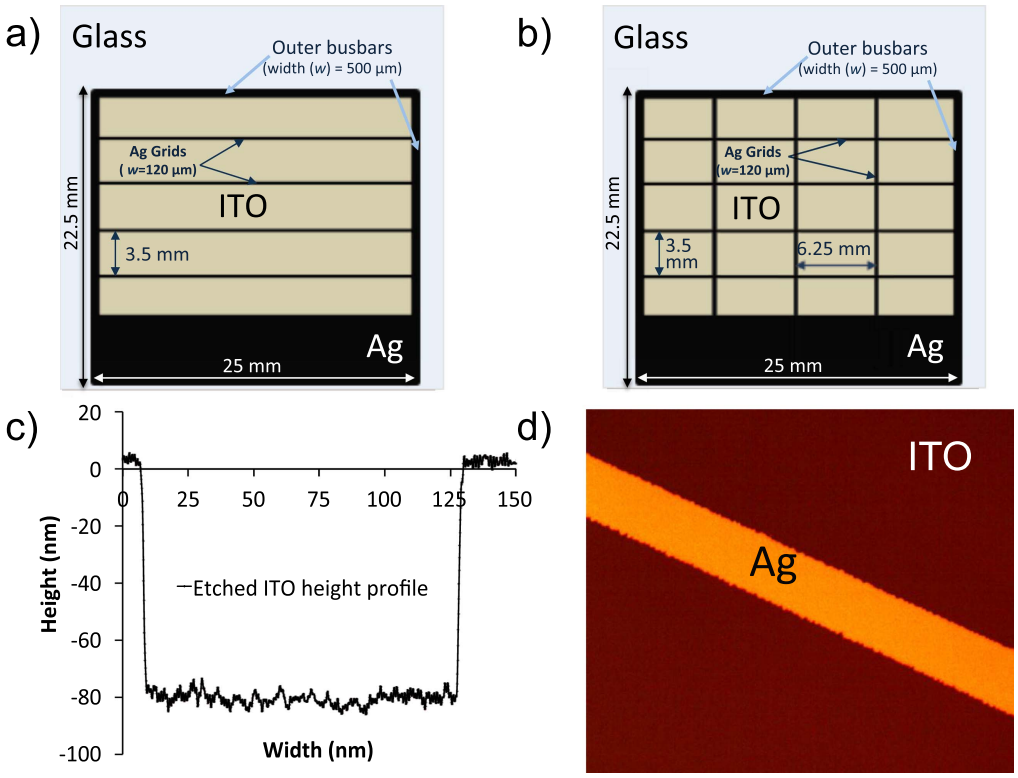

Figure 3. Schematics showing the dimensions of Ag grids with (a) line pattern and (b) square pattern embedded in the ITO coated glass substrates; (c) the height profile of the etched grid region in ITO after stripping off the photoresist; and (d) an optical microscope image of an Ag grid embedded in ITO on glass.

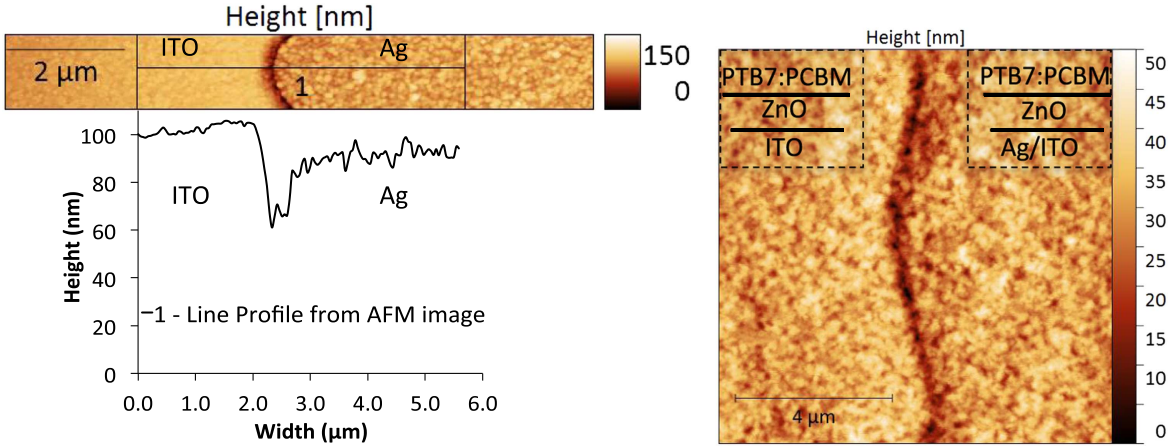

Figure 4. (*Top left*) AFM image (10 × 1 μm) of an intersection between embedded Ag grid and ITO. (*Bottom left*) Line profile from the AFM image showing height profile of the intersection between embedded Ag grid and ITO. (*Right*) An AFM image showing the topography of the PTB7:[70]PCBM blend coated on ZnO layer at the intersection of the embedded Ag grids in ITO.

Figure 4 (*left*) shows an AFM image and height profile of an intersection between embedded Ag grid and ITO. A horizontal gap of approx. 500 nm between the evaporated Ag grid and ITO can be observed from the line profile. This gap arises due to the undercut during the negative lithography process and subsequent isotropic ITO etching [32]. The gap can affect the subsequent device fabrication part negatively, and thus lower the overall device yield, which in turn can be avoided by carefully optimization of the lithography parameters. In our case, it is expected that this gap is filled up and planarized due to capillary action while coating ZnO as well as PTB7:[70]PCBM solution blend on top of the electrodes. The topography of the PTB7:[70]PCBM active layer at the ITO-Ag intersection on the ZnO coated electrodes is shown in AFM image in figure 4 (*right*), demonstrating no detectable morphology difference between the two regions.

The average sheet resistance of the 100 nm thick ITO layer was ~20 Ω/Sq., while the electrodes with the embedded Ag grids with line and square pattern in ITO demonstrate average sheet resistance values of ~15 Ω/Sq. and ~12 Ω/Sq., respectively. The relatively large drop in sheet resistance here should have a clear effect on the device performance,

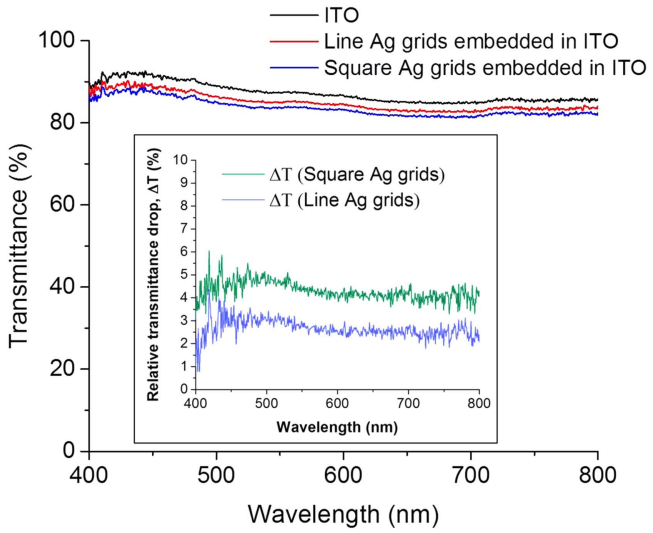

Figure 5. The transmission spectra of ITO and embedded Ag grids in ITO (excluding busbars) on glass in the visible light region; (*inset*) relative drop in transmittance, ΔT (measured excluding busbars) of ITO after embedding Ag grids in ITO.

particularly due to an improved FF. The sheet resistance of the embedded Ag grids in ITO with square pattern is lower compared to that of Ag grids with line pattern. However, the line pattern of the embedded Ag grids keeps the transmittance of the electrodes comparatively higher than the transmittance of square grids due to less coverage of Ag grids. The total area coverage of the line and square patterned Ag grids on the active cell area was approx. 8% and 11% including the outer busbars, respectively. This is justified from the transmittance spectra taken (figure 5) of the ITO with embedded Ag grids in comparison to the plain ITO electrodes. The average optical transmittance of the plain ITO layer was ≈87%, while for the embedded Ag grids in ITO with line and square pattern (excluding the outer busbars) was around 84% and 82%, respectively. For square grid pattern, the relative transmittance drop in the visible range (ΔT, shown in the inset of figure 5) was comparatively higher than the line grid pattern. This can have direct impact on the short-circuit current density (J_{SC}) of the devices.

Figure 6 (*left*) shows the schematic of the layer stack of the fabricated large area OSCs on the embedded 70 nm Ag grids in 100 nm thick ITO layer on glass. Figure 6 (*right*) shows the JV characteristic comparison of OSCs fabricated with active areas of 4.38 cm^2 fabricated on plain ITO and on ITO with embedded Ag grids, as semi-transparent bottom electrodes. The performance parameters of the fabricated OSCs are summarized in table 1.

For the OSCs on ITO, the FF was 41.7 ± 1.4%, while the FF of the OSCs with the ITO embedded line and square patterned Ag grids were 49.3 ± 1.5% and 54.2 ± 1.4% respectively. The low FF of the reference OSCs arises due to the high sheet resistance of the electrodes, which leads to high series resistance in the large area devices [33, 34]. The series resistances of the OSCs were calculated by linear fitting of the dark JV characteristics (see figure 7). As the series resistance is dominant in the high voltage region [35], the dark JV curves were linearly fitted in the region of 800–1000 mV. The inverse of the slope (m) to the linear fit, $y = mx + b$, of the dark JV curves provided the series resistance of the devices, which was reportedly, 39.1 Ω cm^2, 17.3 Ω cm^2 and 15.0 Ω cm^2 for the plain ITO and ITO with embedded line and square patterned Ag grids, respectively.

The decrease in series resistance for devices including the Ag grids embedded in the ITO layer leads to the increase in the FF values, resulting in the overall increase in PCE. Hence, for the OSCs on ITO with embedded line and square patterned Ag grids as bottom electrodes, the measured values of the FF were 18% and 30% higher, respectively, than the FF of the reference OSCs on pure ITO bottom electrodes. Slight improvements in V_{OC} can be observed for the OSCs having embedded Ag grids due to modified interface effects induced by the lower work function embedded Ag compared to pure ITO.

The J_{SC} of OSCs with the line and square patterns however, do not change much. The observed J_{SC} of the fabricated OSCs on embedded line patterned Ag grids is almost similar to that of the reference ITO (within error bars the same). However, for the OSCs with square Ag grids, the J_{SC} drops compared to the reference OSCs. The reason for this drop is due to the coverage of the embedded Ag grids in ITO. The line grid patterns covers 8% and the square grid patterns covers 11% of the total active area, resulting in less excitons generated in the active layer of the square patterned cell due to the larger shadow effects. The decreased series resistance compensating this effect could explain the reason why a J_{SC} decrease is not observed for the line patterns.

4. Conclusion

100 nm thick ITO coatings on glass substrates were patterned by a standard photolithography process and wet etched up to 80 nm. A following E-beam evaporation process filled the etched grid lines with 70 nm Ag on top of an ultrathin Ti adhesion layer. Embedding the Ag grids in ITO reduces the sheet resistance of large area ITO electrodes from 20 Ω/Sq. to 15 Ω/Sq. for line grid pattern and to 12 Ω/Sq. for the square grid pattern. The average optical transmittance of the embedded Ag grids is <6% lower than the transmittance of the plain ITO. Inverted bulk heterojunction OSCs based on PTB7:[70]PCBM blend with cell area of 4.38 cm^2 were fabricated on these electrodes. Because of the decreased sheet resistance of the ITO electrodes with embedded Ag grids, the FF of the OSCs based on these electrodes increased by 18% and 30%, respectively, for the line and square Ag grid patterns, compared to that of the reference OSCs on plain ITO. A maximum FF of 54.2 ± 1.4 was achieved by embedding square patterned Ag grids in ITO. However, the PCE of the OSCs with the line and square embedded Ag grid patterns remain the same. This is due to the drop in J_{SC} for the OSCs with the embedded square patterned grid electrodes arising from shading effects due to the higher coverage of Ag grids in this configuration. With further modifications in the design of the Ag grids patterns embedded in ITO, it is expected that the

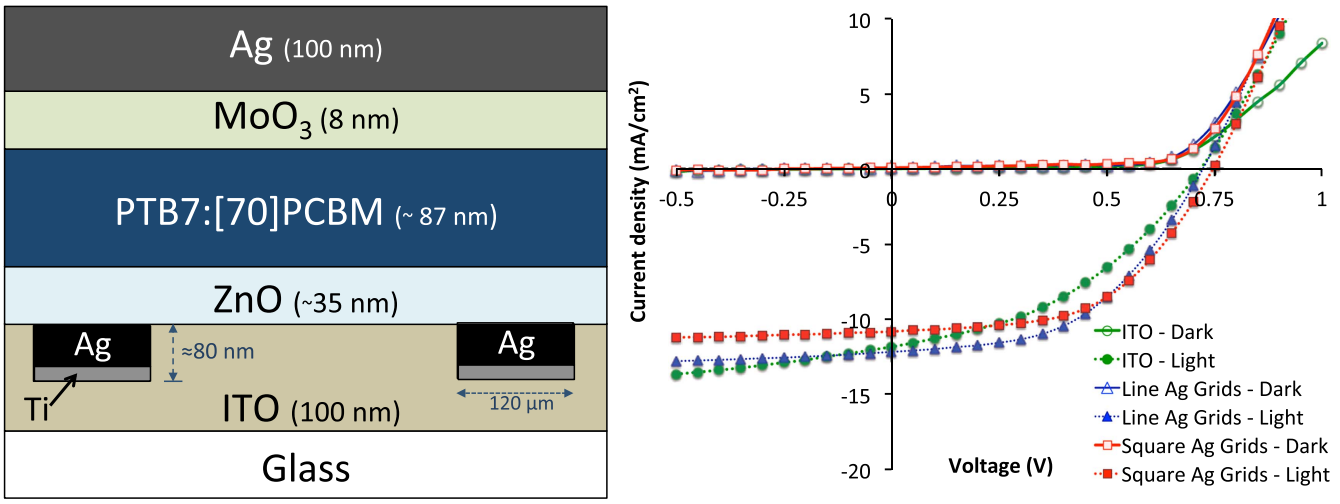

Figure 6. (*Left*) The layer stack schematic of the fabricated large area OSCs with 70 nm embedded Ag grids in 100 nm thick ITO layer on glass. 3 nm of Ti was used as adhesion layer between Ag and ITO. (*Right*) JV characteristics comparison of the OSCs under dark and light with cell area of 4.38 cm^2, fabricated on ITO as well as on ITO with embedded line and square Ag grids as semi-transparent electrodes.

Table 1. Performance parameters of the fabricated OSCs with and without the embedded Ag grid lines.

Semi-transparent bottom electrode	Sheet resistance (Ω/Sq.)	Series resistance (Ω cm^2)	V_{OC} (mV)	J_{SC} (mA cm^{-2})	FF (%)	PCE (%)
ITO	20	39.1	715 ± 3	11.8 ± 0.2	41.7 ± 1.4	3.52 ± 0.10
Line Ag grids in ITO	15	17.3	722 ± 5	12.2 ± 0.3	49.3 ± 1.5	4.32 ± 0.04
Square Ag grids in ITO	12	15.0	739 ± 6	10.8 ± 0.2	54.2 ± 1.4	4.34 ± 0.15

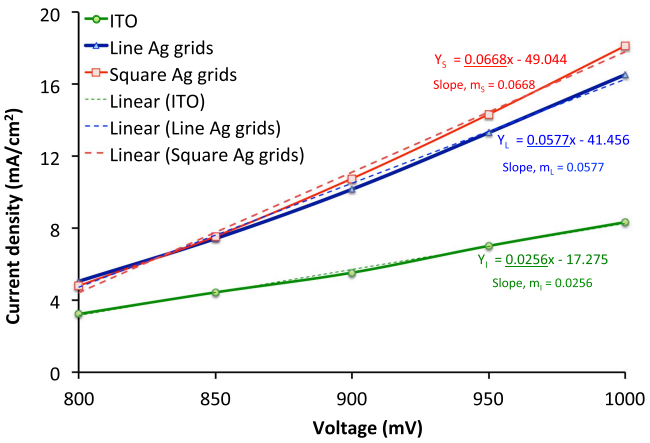

Figure 7. Calculation of the series resistance by linear fitting the dark JV characteristics of the OSCs. The slope (m) was calculated from the linear equation $y = mx + b$; the inverse of the slope is given as the series resistance.

sheet resistance of the ITO layer could be further decreased, leading to further improvement in the device performance. In the presented approach, the processes involved in embedding the Ag grids in ITO coatings did not involve high temperature processes, and this method for increasing the conductivity of ITO can easily be utilized in the fabrication of large area electrodes for highly efficient OSCs on solvent resistant, flexible substrates, for which high temperature based processes are not suitable.

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